

# H61MXE-V(H61M06)Fab A

Micro ATX 8.9X6.8

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- H61MXE-S    USB3+RTL8111F+POWER MOS+Solid CAP
- H61MXE        RTL8111F
- H61MXE-V    RTL8105E

CPU:

Intel Sandy Bridge processors in LGA1155 Package

System Chipset:

PCH

Main Memory:

Dual Channel / DDR-III \* 2 (Max 8GB)

Expansion Slots:

PCI EXPRESS 16X SLOT \*1

PCI EXPRESS 1X SLOT \* 2

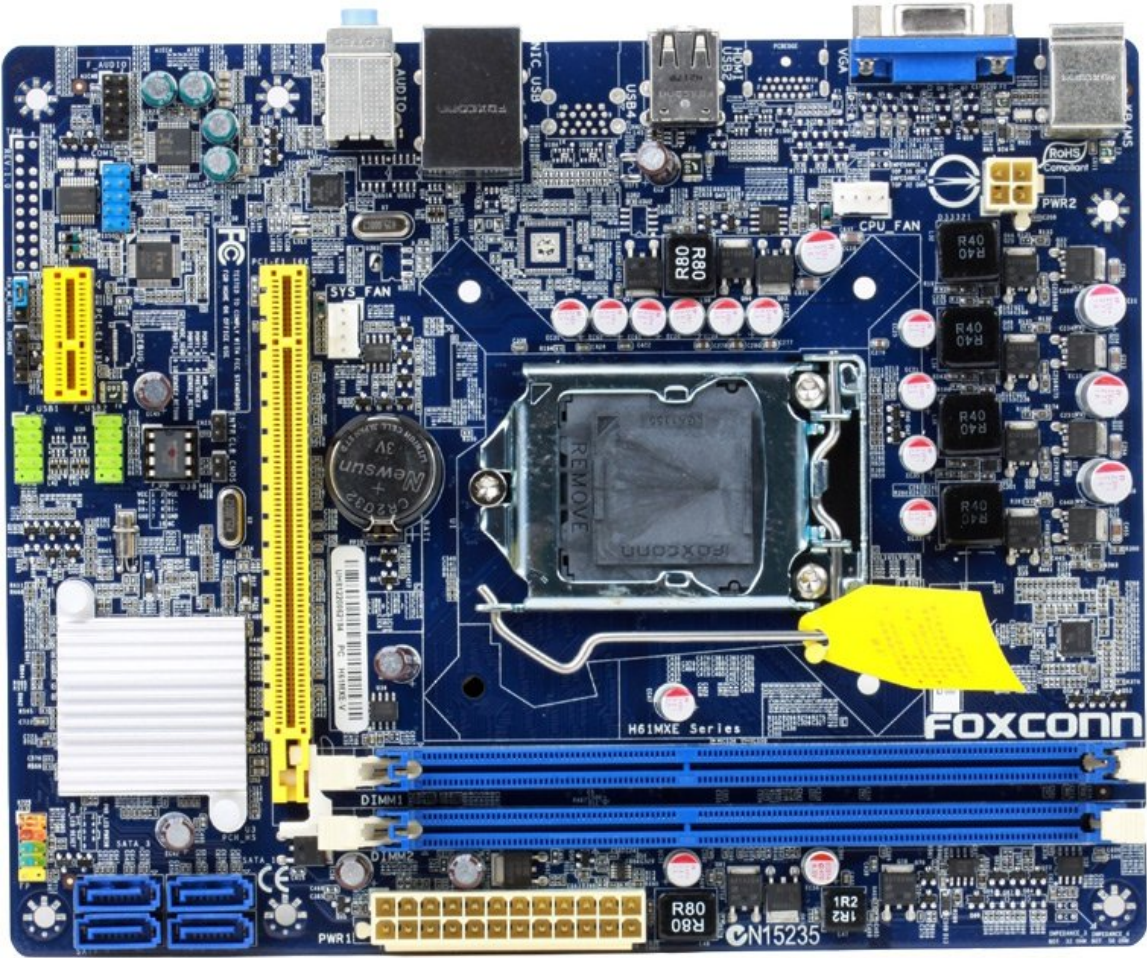
On Board Device:

SIO: IT8772

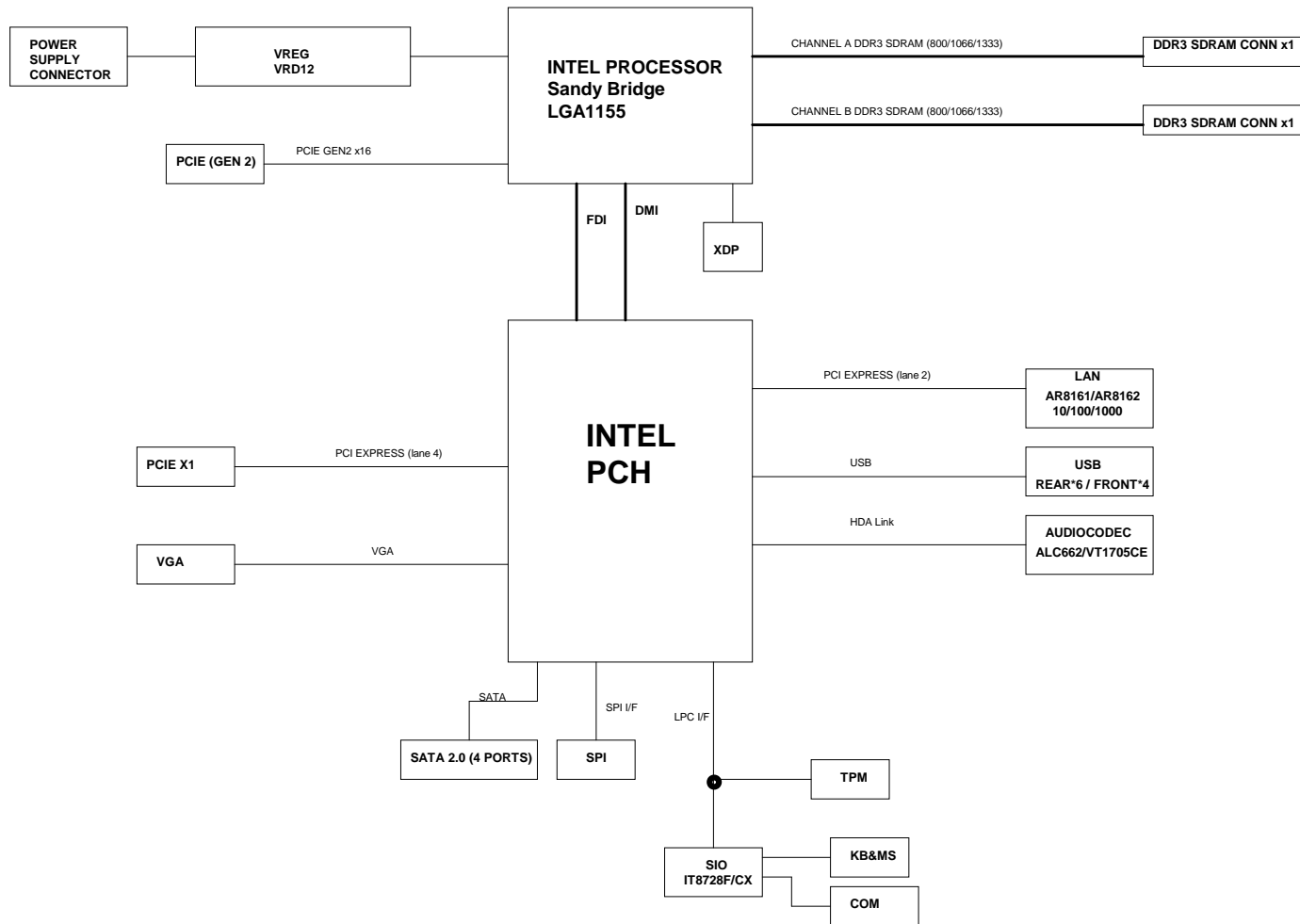
LAN: ReITek RTL8111F/8105E

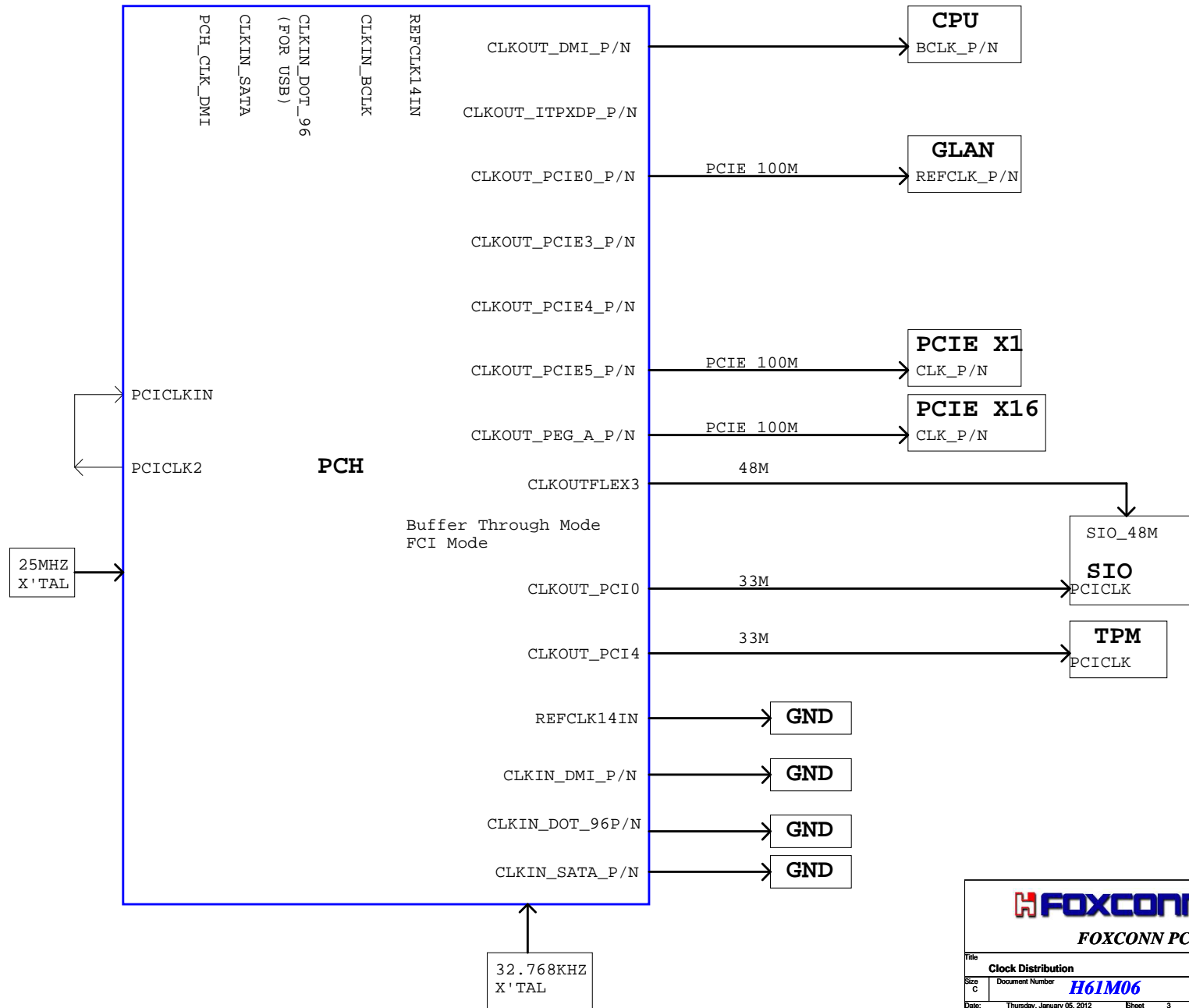
HDA Codec: ALC662

BIOS:SPI Flash ROM 4Mbyte

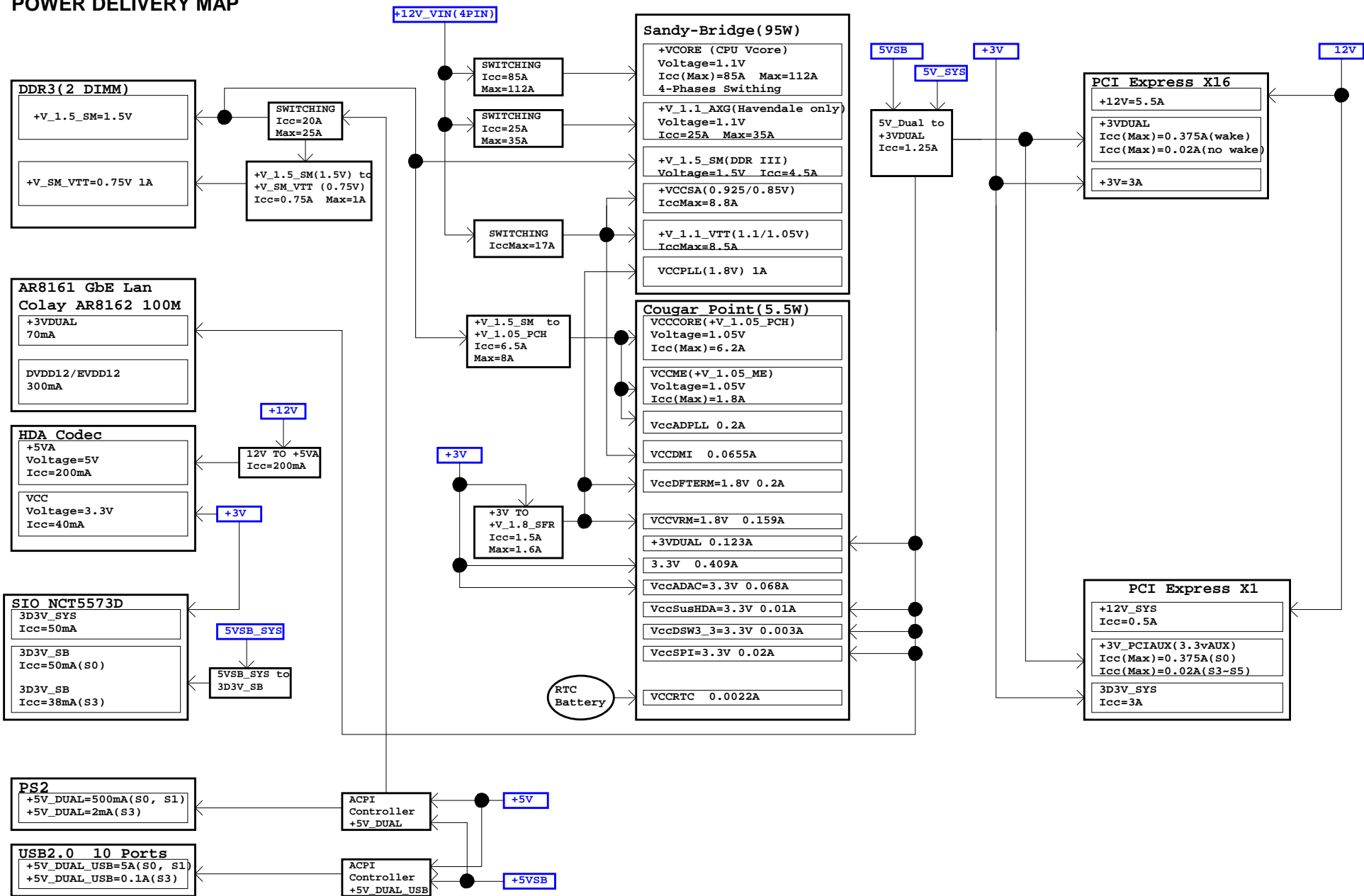


## BLOCK DIAGRAM





# POWER DELIVERY MAP



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Title <b>Power Delivery Map</b>		
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POWER ON SEQUENCE

G3 w/RTC Loss to S4/S5 (Without Deep S4/S5 Support) Timing Diagram

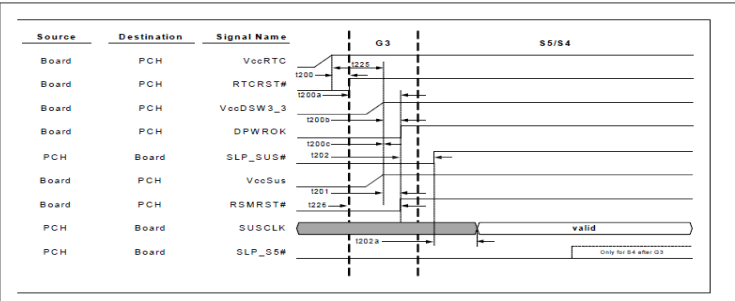


Figure 8-4. S3/M3 to S0 Timing Diagram

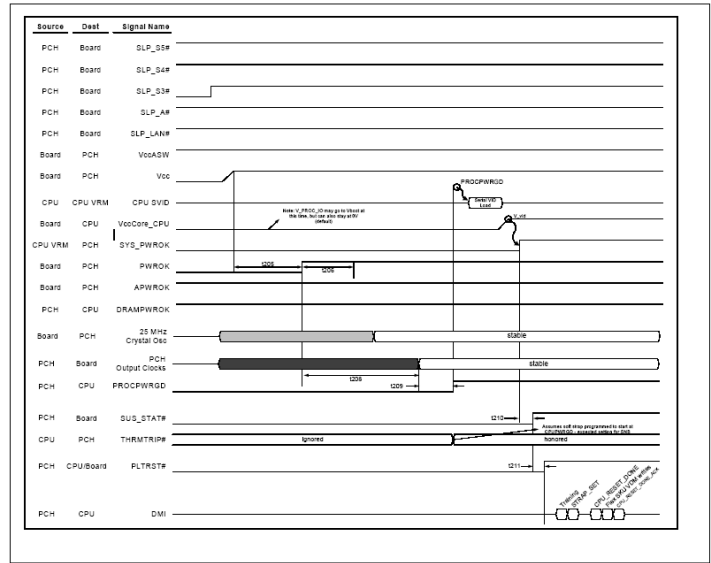


Figure 8-8. DRAMPWROK Timing Diagram

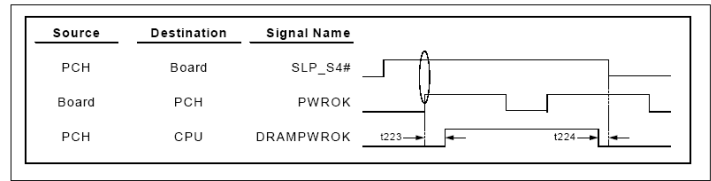


Figure 8-3. S5 to S0 Timing Diagram

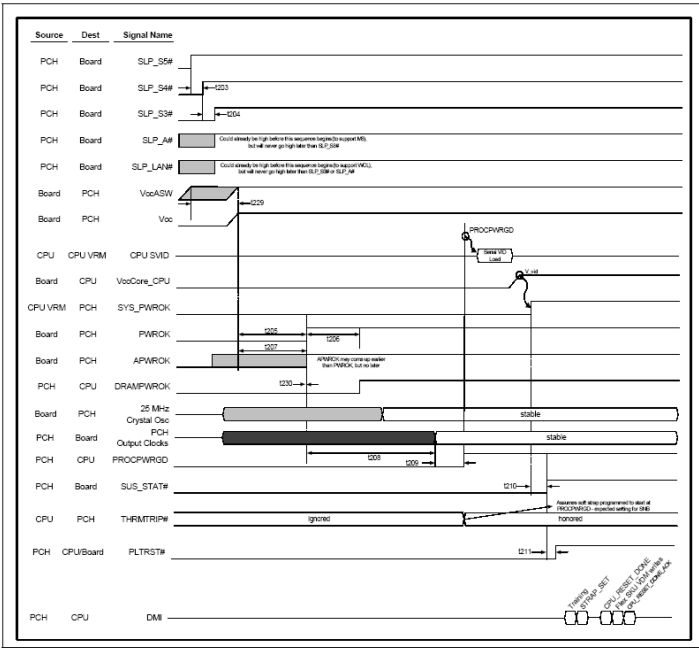
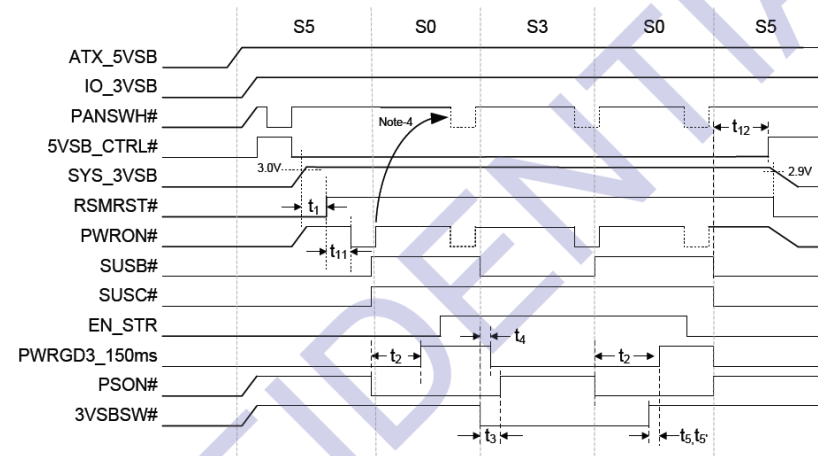


Figure 11-16. EuP Function Signal Timings



## RESET / Power Good MAP

### Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWRGD
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWRGD D3\_RESET#
- (9) H\_PWRGD
- (10) S\_PLTRST# H\_RESET#\_R S\_PLTRST#\_R
- (11) X\_PLTRST\_PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#

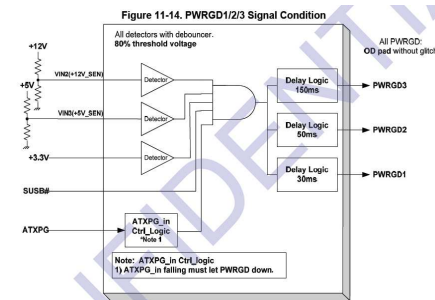
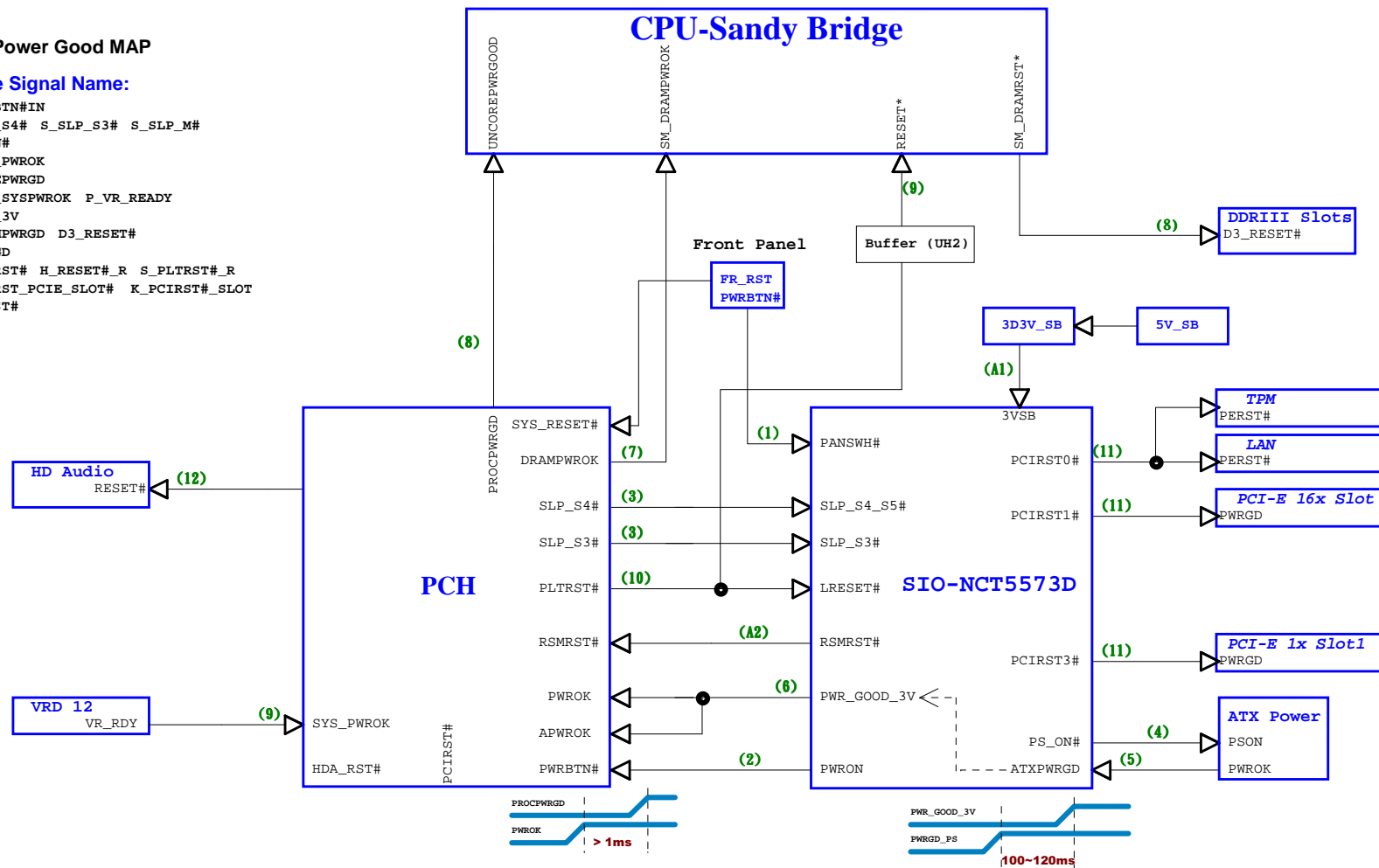


Figure 11-15. PWRGD1/2/3 Signal Timings

IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	16	0	0

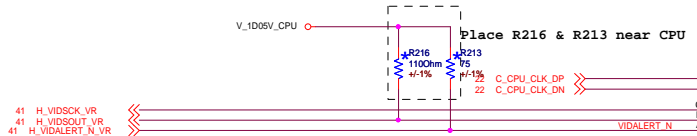
	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	17	2	2

STRAPPING Table

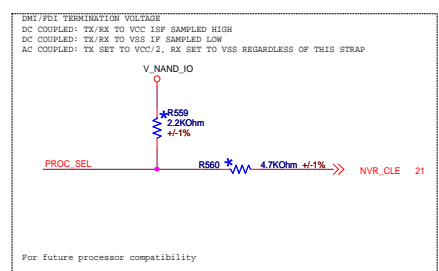
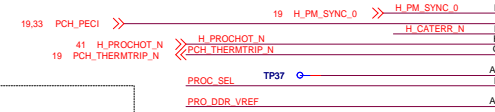
CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

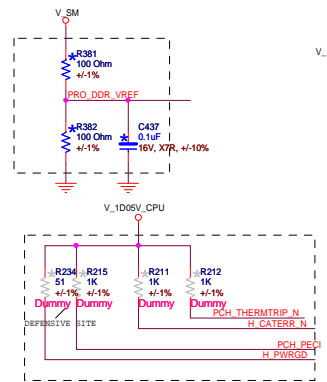




MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SIGNAL PAGE  
PLACE IN CRB AREA



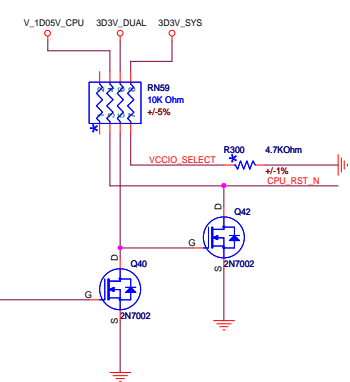
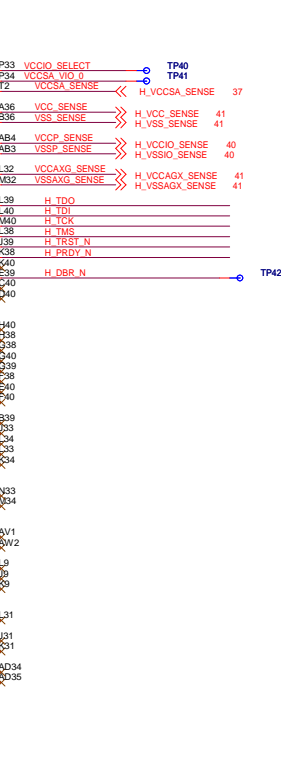
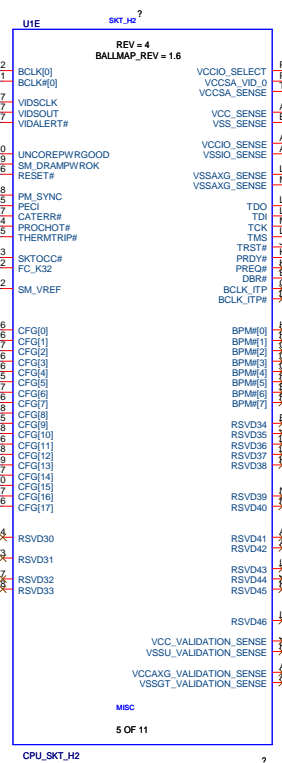
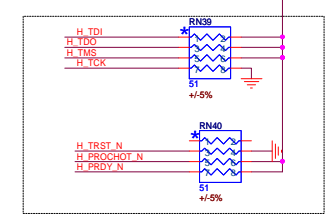
PLACE R381, R382, C437 IN SOCKET CAVITY



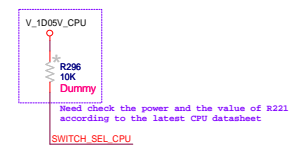
PLACE TDO TERMINATION  
NEAR XDP CONNECTOR

TERMINATION IDEALLY TO BE  
PLACED PLACE CLOSE TO EACH OTHER TO REDUCE STUB  
NEXT TO IT OR WITHIN 1.5 OF CPU.

PLACE TRST\* TERMINATION  
ANYWHERE ON ROUTE.



Need to be double checked.



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File  
**CPU1-MSIC**

Size  
C

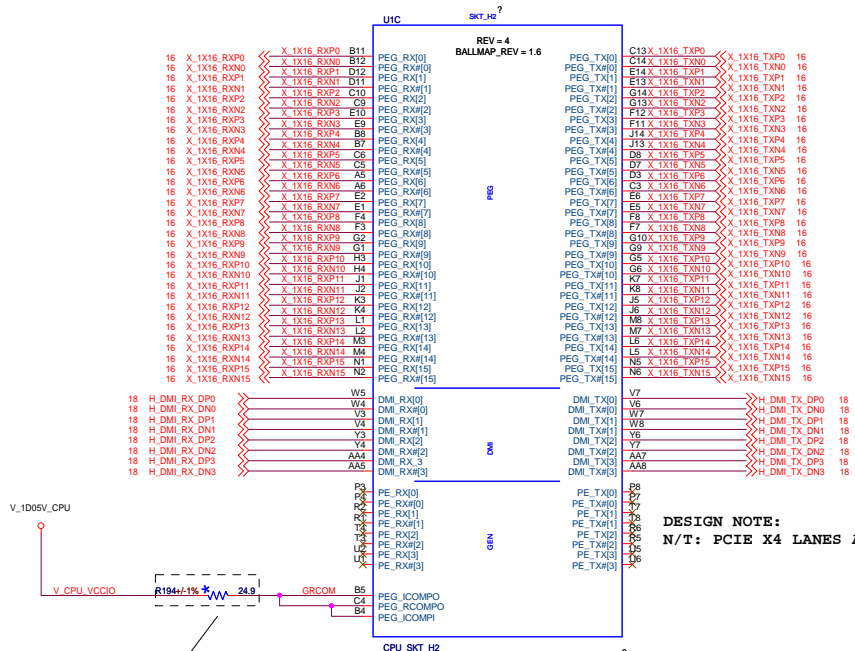
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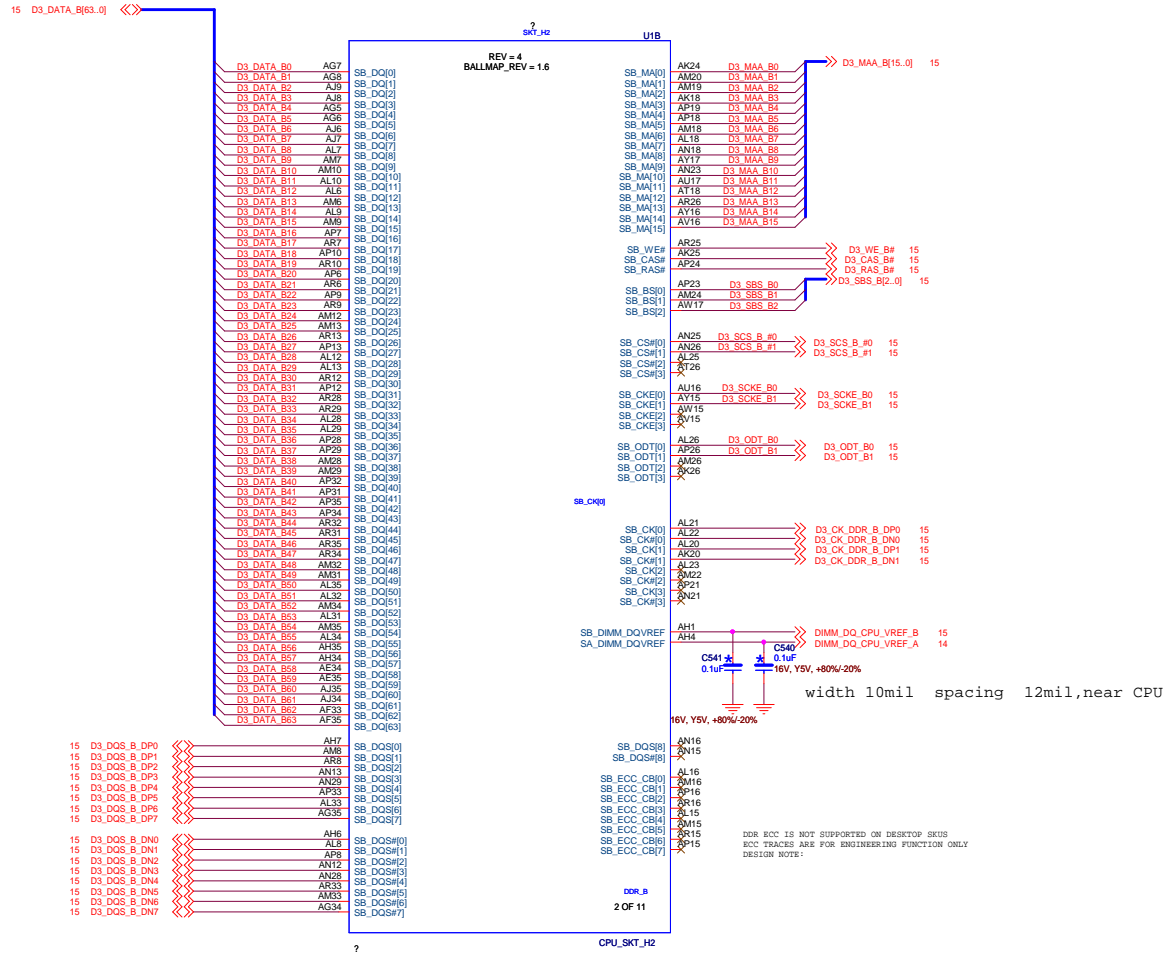
Rev  
A





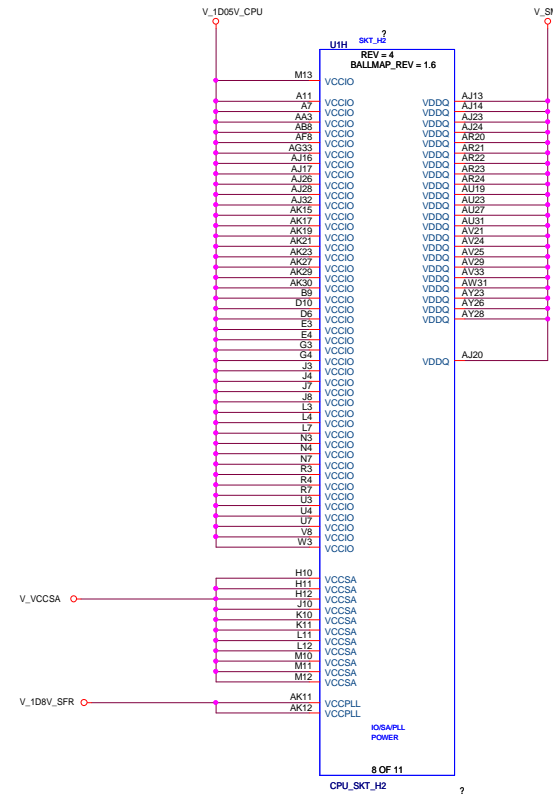
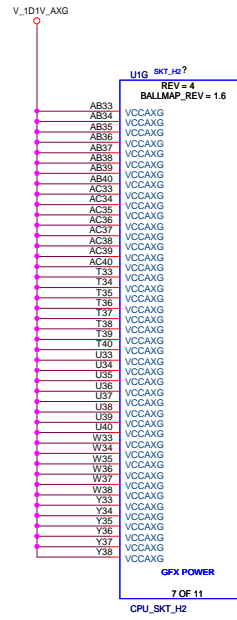
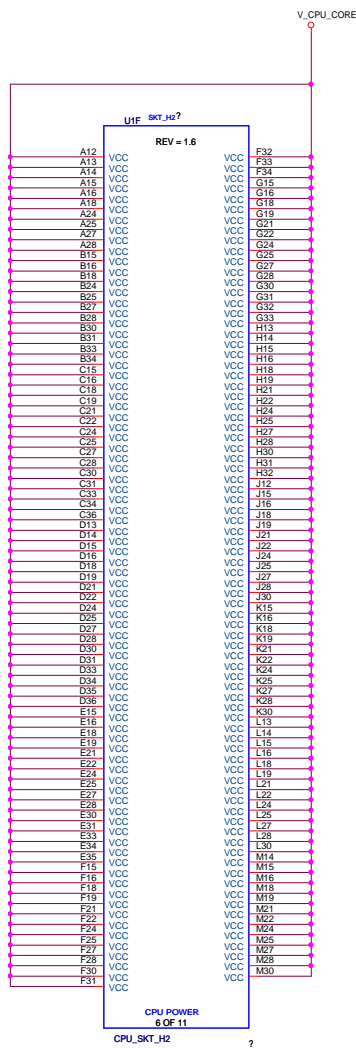
DESIGN NOTE:  
N/T: PCIE X4 LANES ARE NOT SUPPORTED ON DESKTOP CPU SKUS



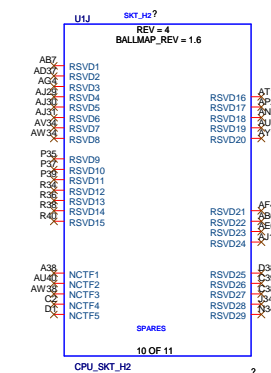
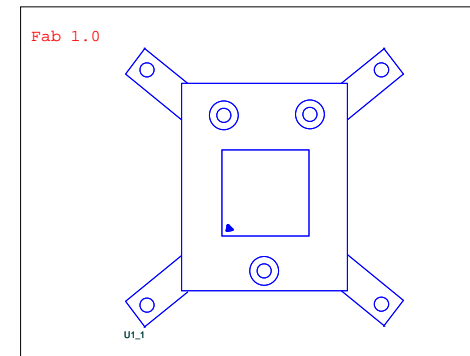
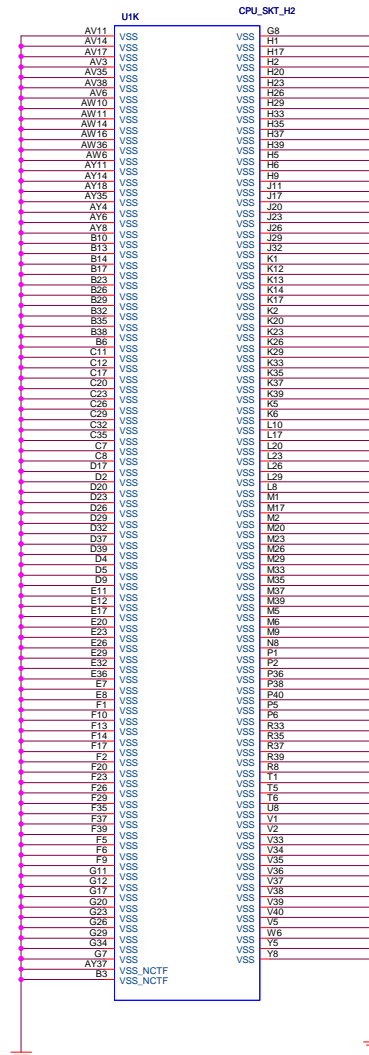
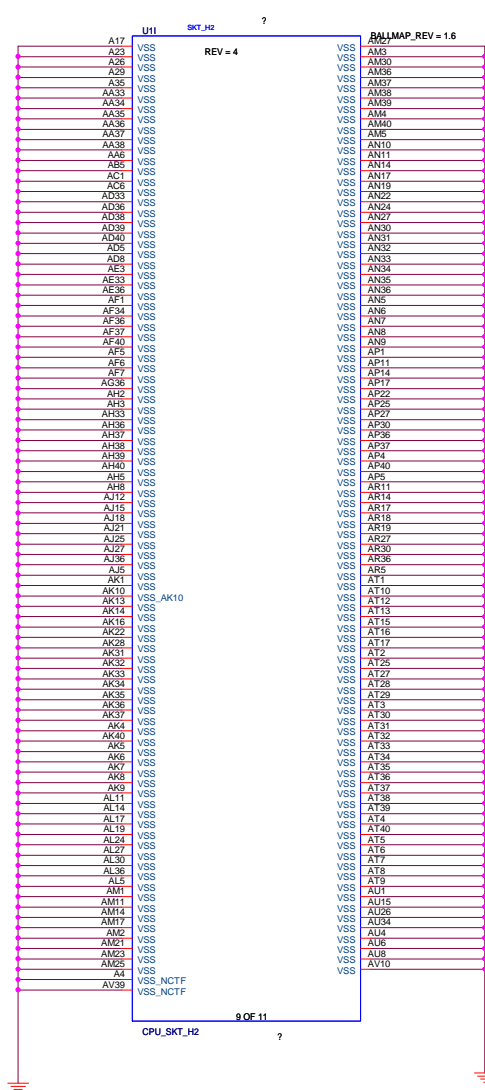


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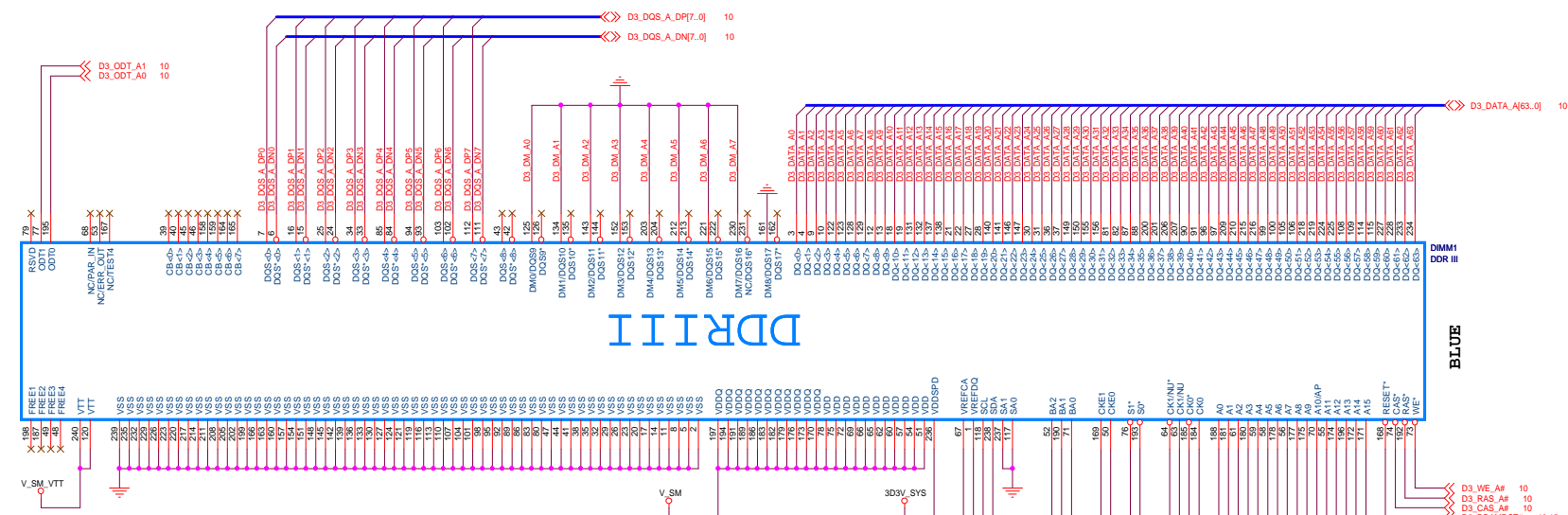


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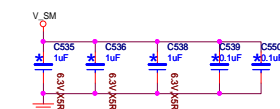


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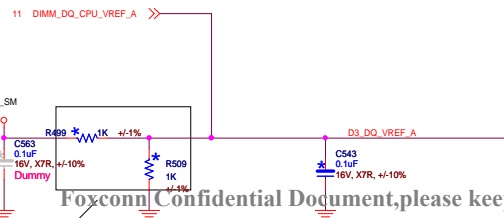
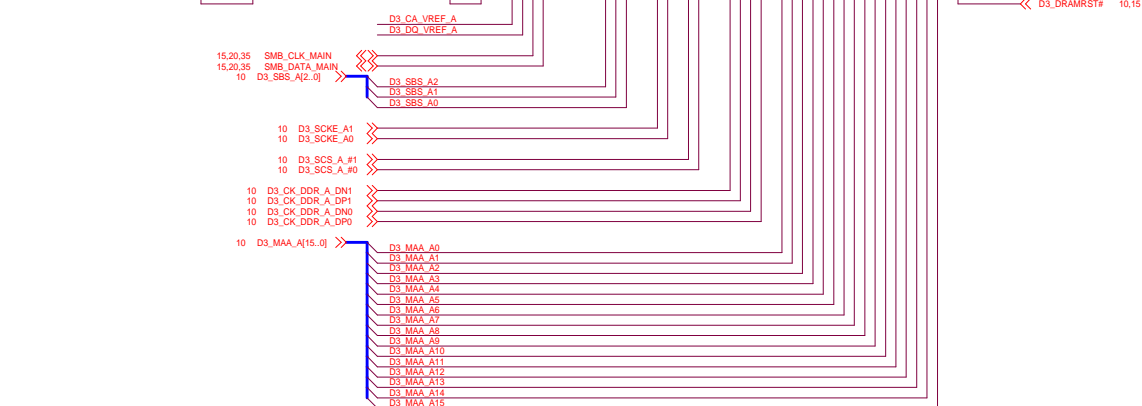
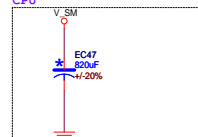
CHANNEL A DIMM 1  
SMB ADDRESS:000



CLOSE TO DIMM POWER PIN



PLACE BETWEEN DIMM1 AND  
CPU

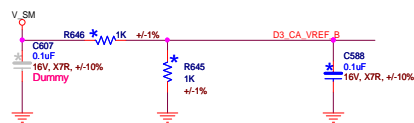


PLACE RESISTORS CLOSE TO CH\_A DIMMS  
ON DIMM\_VREF\_A

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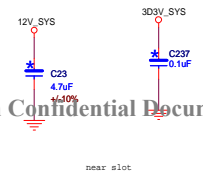



Title			
DDR3-1:CHA			
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PLACE RESISTORS CLOSE TO CH\_B DIMMS  
ON DIMM\_VREF\_B

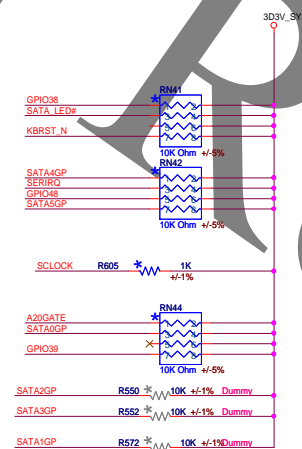
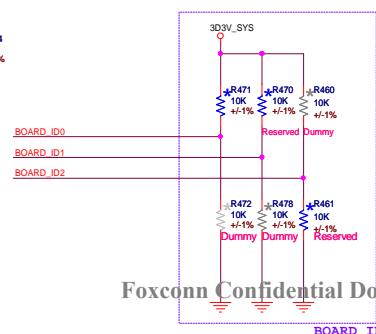
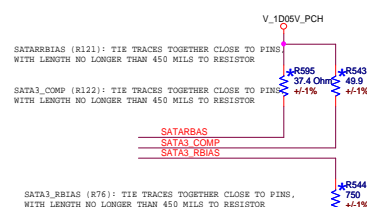
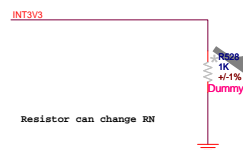
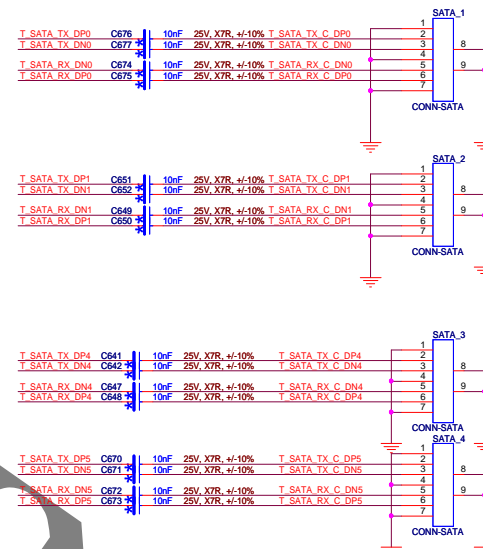




			
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PCIE X16/X1			
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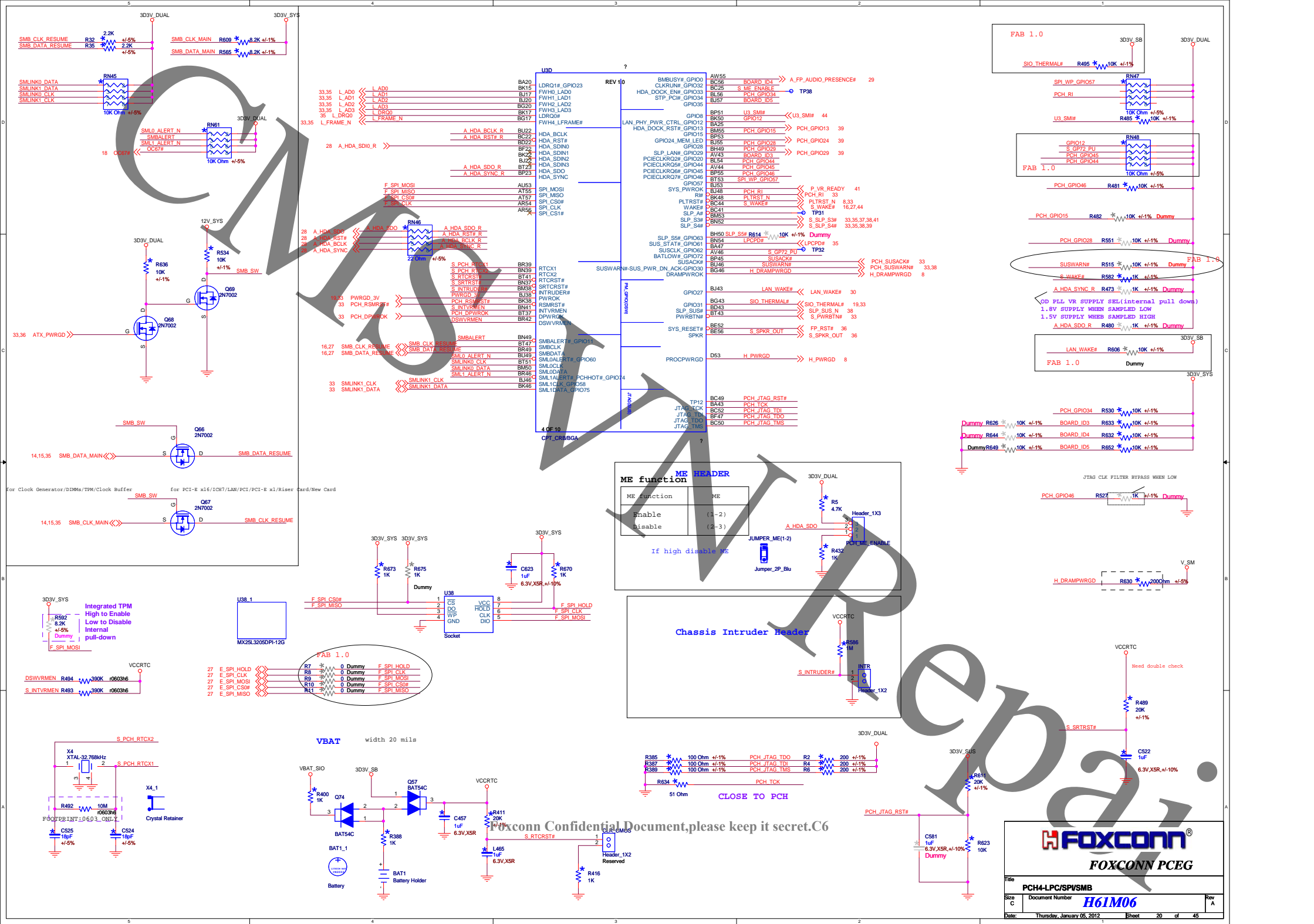






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<b>H61MXE-V</b>	<b>0</b>	<b>1</b>	<b>1</b>

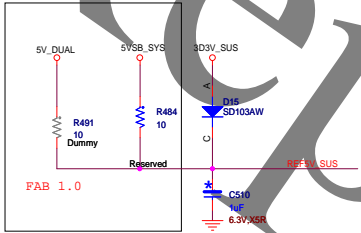
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USU CPT\_CRB

REV 1.0

BC15 VSS\_125  
BC20 VSS\_126  
BC27 VSS\_127  
BC31 VSS\_128  
BC36 VSS\_129  
BC38 VSS\_130  
BC47 VSS\_131  
BC53 VSS\_132  
BD03 VSS\_133  
BF12 VSS\_134  
BF20 VSS\_135  
BF25 VSS\_136  
BF33 VSS\_137  
BF41 VSS\_138  
BF46 VSS\_139  
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BF6 VSS\_142  
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BG25 VSS\_144  
BG26 VSS\_145  
BG27 VSS\_146  
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BG33 VSS\_148  
BG36 VSS\_149  
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BH6 VSS\_151  
BU1 VSS\_152  
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BU3 VSS\_170  
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BN47 VSS\_172  
BN6 VSS\_173  
BP3 VSS\_174  
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BP36 VSS\_176  
BR22 VSS\_177  
BR52 VSS\_178  
BU19 VSS\_179  
BU26 VSS\_180  
BU29 VSS\_181  
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BU39 VSS\_183  
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AY38 VSS\_221  
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BA49 VSS\_100  
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M8 VSS\_112  
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N54 VSS\_114  
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R17 VSS\_117  
R22 VSS\_118  
R4 VSS\_119  
R41 VSS\_120  
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R46 VSS\_122  
R49 VSS\_123

USL

L12 VSS\_231  
L17 VSS\_232  
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L43 VSS\_235  
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M22 VSS\_237  
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U53 VSS\_254  
V20 VSS\_255  
V38 VSS\_256  
V6 VSS\_257  
W1 VSS\_258  
W55 VSS\_259  
W57 VSS\_260  
Y11 VSS\_261  
Y15 VSS\_262  
Y38 VSS\_263  
Y40 VSS\_264  
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Y49 VSS\_268  
Y52 VSS\_269  
Y6 VSS\_270

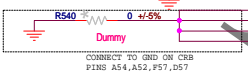
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A6 VSS\_NCTF\_2  
B2 VSS\_NCTF\_3  
BM1 VSS\_NCTF\_4  
BM57 VSS\_NCTF\_5  
BP1 VSS\_NCTF\_6  
BT2 VSS\_NCTF\_7  
BU4 VSS\_NCTF\_8  
BU52 VSS\_NCTF\_9  
BU54 VSS\_NCTF\_10  
BU6 VSS\_NCTF\_11  
D1 VSS\_NCTF\_12  
F1 VSS\_NCTF\_13  
VSS\_NCTF\_14

AY22 VSS\_231  
C12 VSS\_232  
AE56 VSS\_233  
BR36 VSS\_234  
AU2 VSS\_235

A54 VSS\_236  
A52 VSS\_237  
F57 VSS\_238  
D57 VSS\_239

CPT\_CRB/BGA

L33 TP3  
2E49 TP13  
2Y36 TP17  
2Y14 TP18  
2Y12 TP19  
2Y22 TP20  
2Y38 TP1  
P25 TP4  
R25 VSS\_206  
P36 VSS\_206  
R36 VSS\_204  
L31 VSS\_200  
2Y6 TP2  
TP5 VSS\_263  
VSS\_264 VSS\_264  
VSS\_291 VSS\_291  
AE41 TP14  
2E43 TP15  
BA27 TP11  
BM46 TP10  
AG12 L\_BKLTCTL  
2C18 L\_BKLTEN  
AG17 L\_VDD\_EN



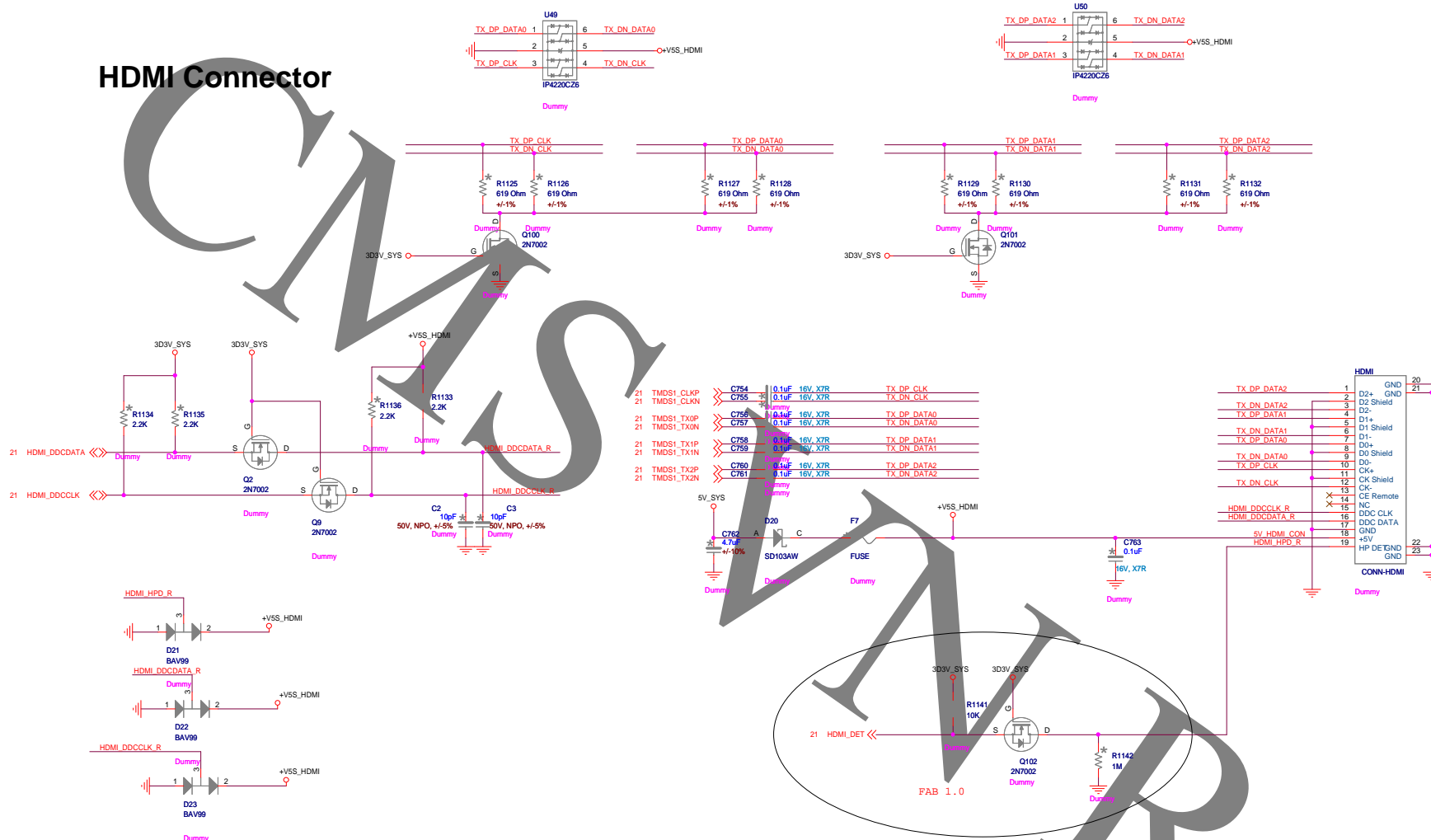
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Title		
PCH7-GND		
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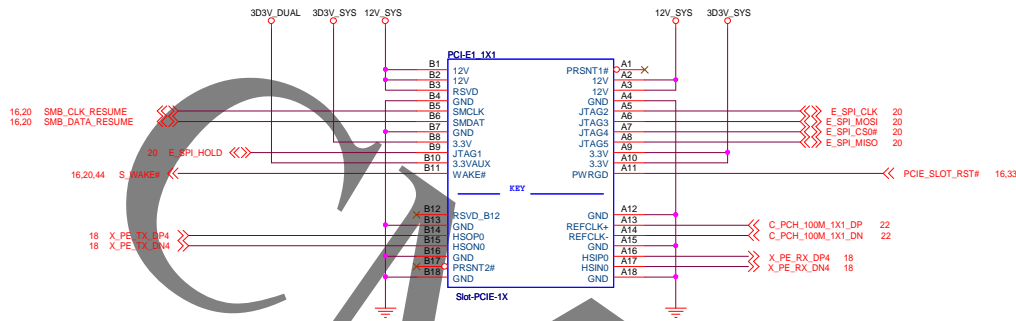


# HDMI Connector



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 <b>FOXCONN PCEG</b>		
File		
DVI		
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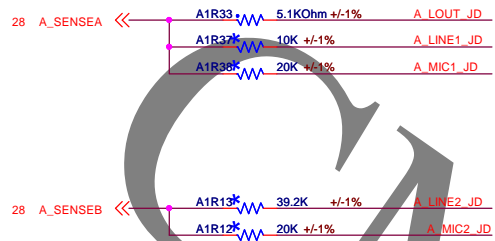


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<b>FOXCONN®</b>		
<b>FOXCONN PCEG</b>		
Title		
<b>PCIE 1X</b>		
Size	Document Number	Rev
C	<b>H61M06</b>	A
Date:	Thursday, January 05, 2012	Sheet 27 of 45

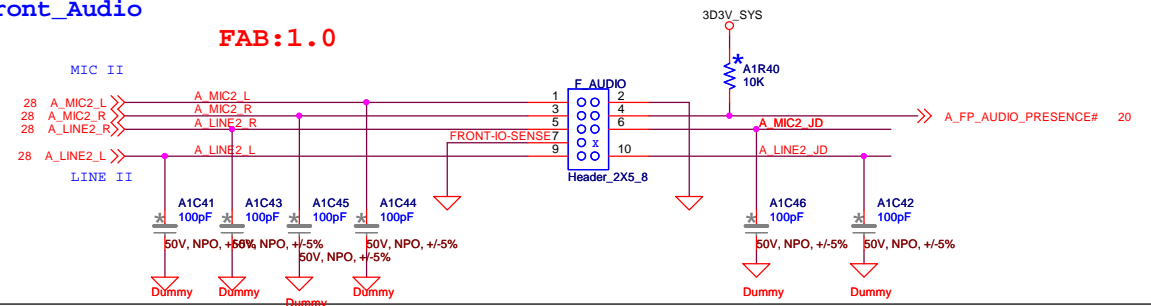


## JACK SENSE



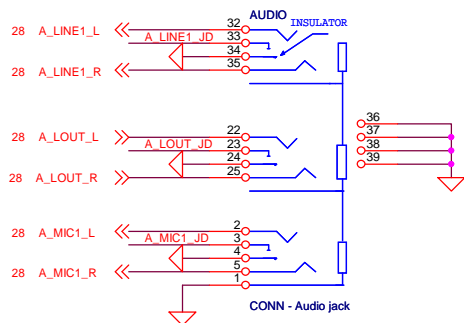
## Front\_Audio

FAB:1.0



## +5VA for AUDIO

## Audio Jack



## Audio Jack



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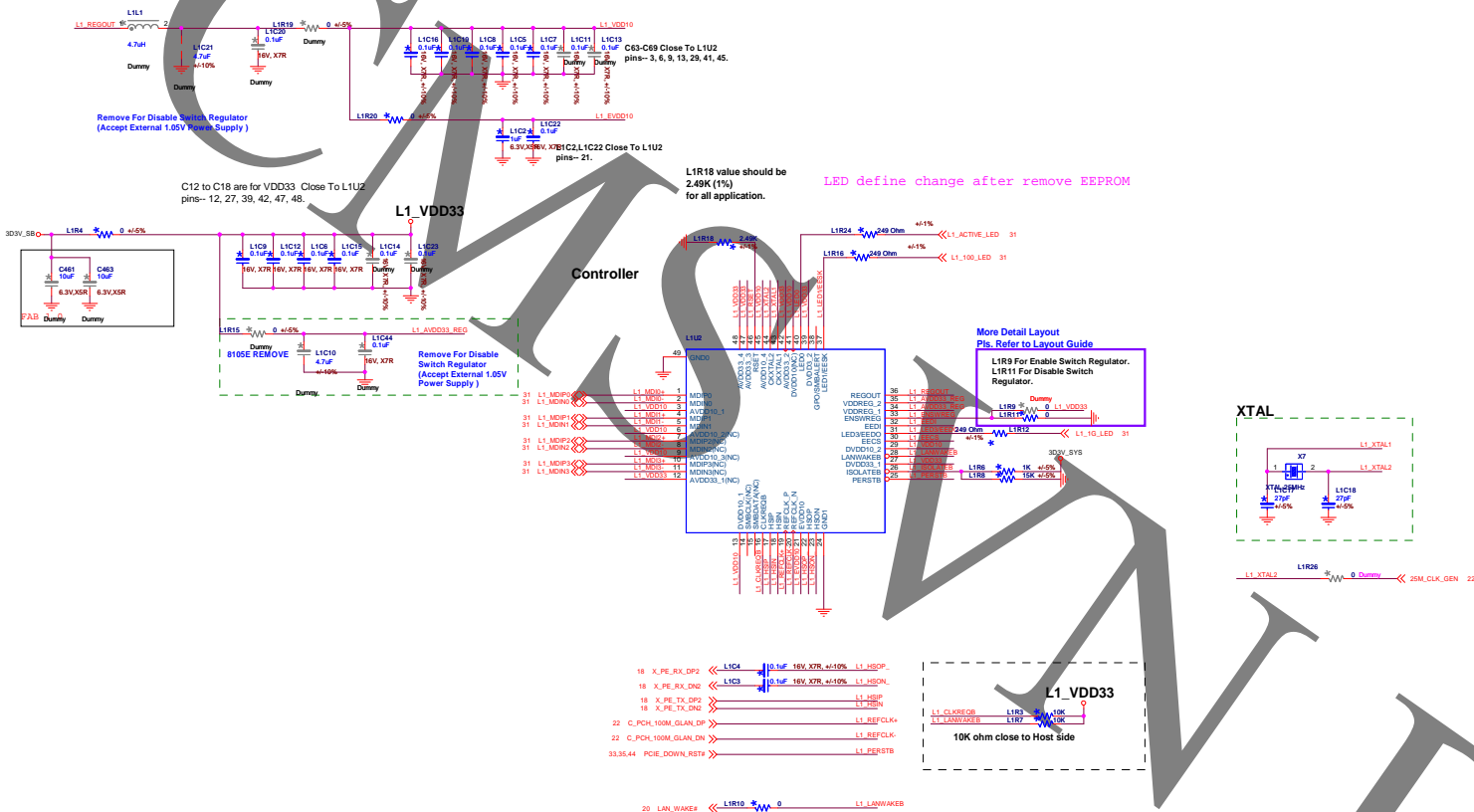
**FOXCONN**

FOXCONN PCEG

Title		AUDIO-2:CONNECTOR	
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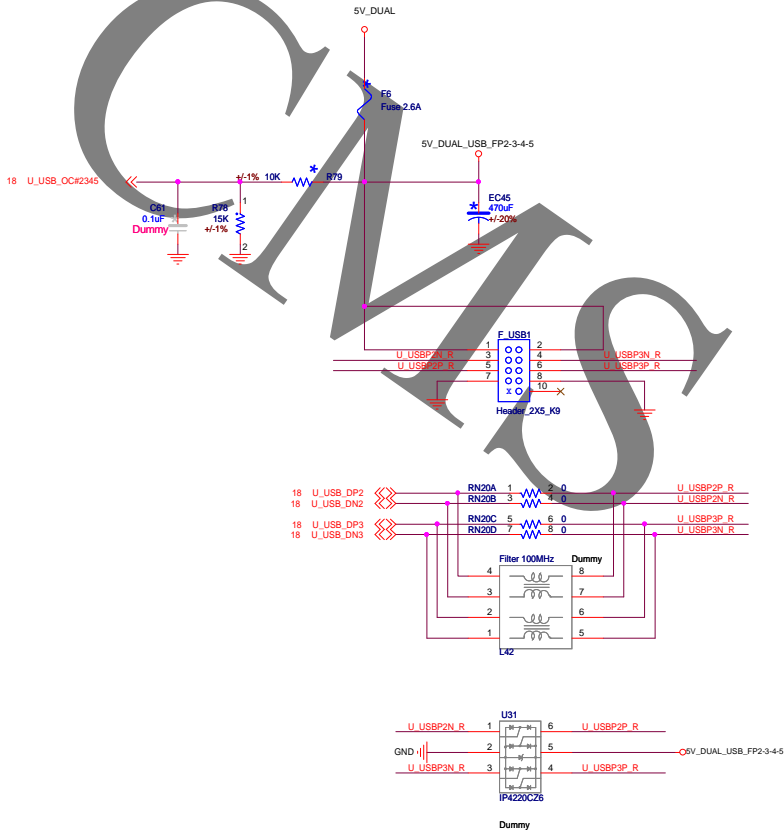
	1.05V / 1.0V source	L1L1	L1C21	L1C20	L1R9/ reserve	L1R11/ reserve
B111E Series/B111F Series/B105E Series	SWR	O	O	O	O	X
B105E Series (except for VL)	LDO	X	X	X	X	O
B111E Series/B111F Series/B105E-VB	External	X	X	X	X	O
B105E Series (except for VB)	External	X	X	X	O	X



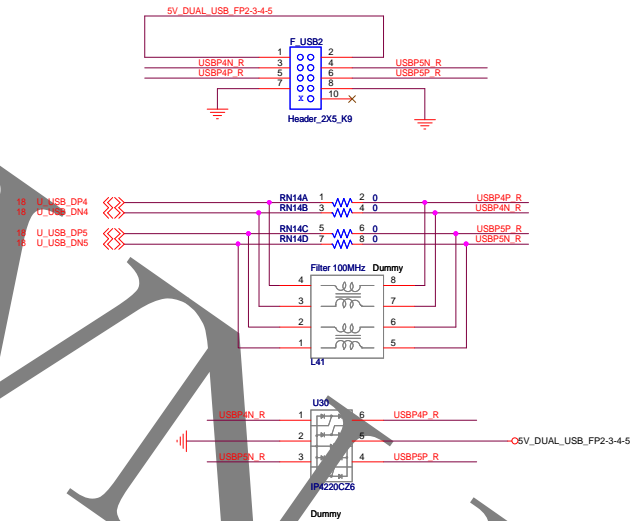
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## Front\_USB1



## Front\_USB2



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 <b>FOXCONN PCEG</b>		
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	Symbol	Value	Description
JP1	DSW_EUP_SEL	0	EUP(default)
Pin-23		0	DSW
JP2	WDT_EN	0	Disable WDT to reset PMKROK(default)
Pin-57		0	Enable WDT to reset PMKROK
JP3	FAN_CTL_SEL	1	EC Index 68h/73h default = 80h
JP4		0	EC Index 68h/73h default = 00h
Pin-59	KSPWR_EN	0	Disable KSPWR Sequence(default)
Pin-61		0	Enable KSPWR Sequence

```

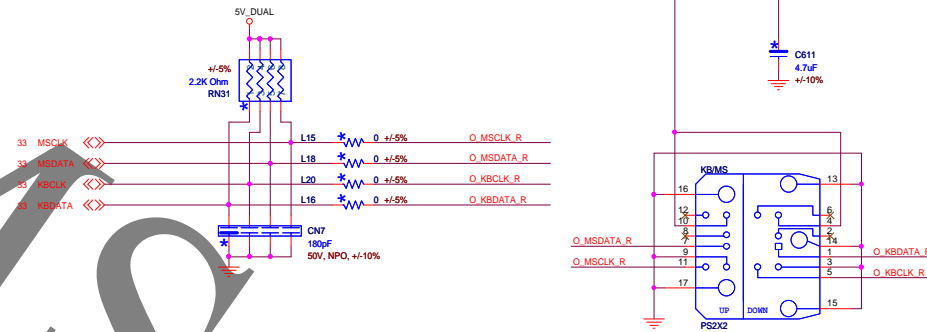
1.Pin 6:ATXPG
2.Pin 30:SUSB#
3.Pin Pin 23 / Pin 57/ Pin 59/ Pin61
4.Pin38-41 KCLK/KDAT/MCLK/MDAT
5.Pin 63 pull high to 3VSB

```



Add for EMI on 0929

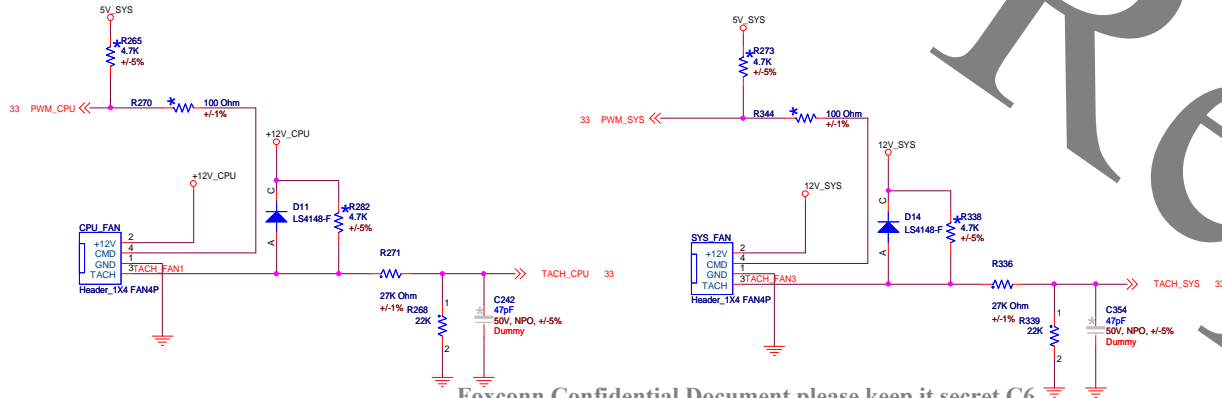
KB /USB connect



CPU FAN

SYS FAN

New FAN Header Definition  
pin1. GND  
pin2. +12V  
pin3. Sense  
pin4. PWM



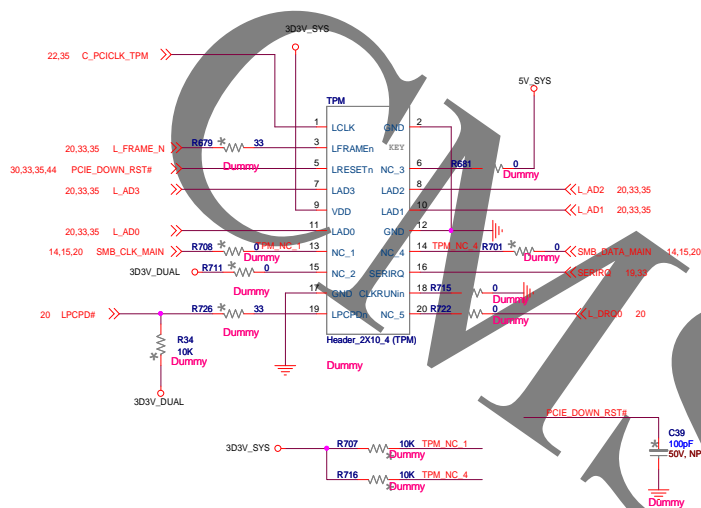
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FOXCONN PCEG

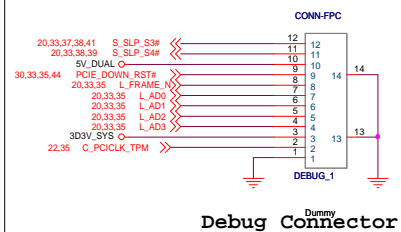
Title: PS2/FAN  
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# TPM



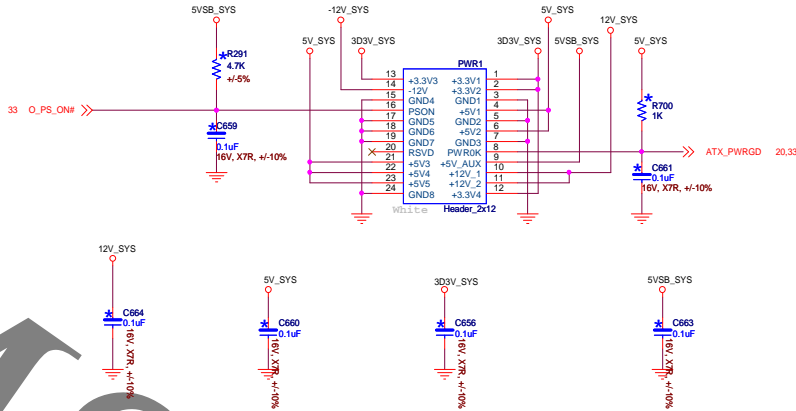
## LPT PORT



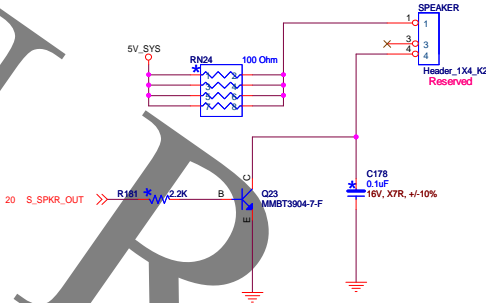
**COM HEADER**

# COM PORT

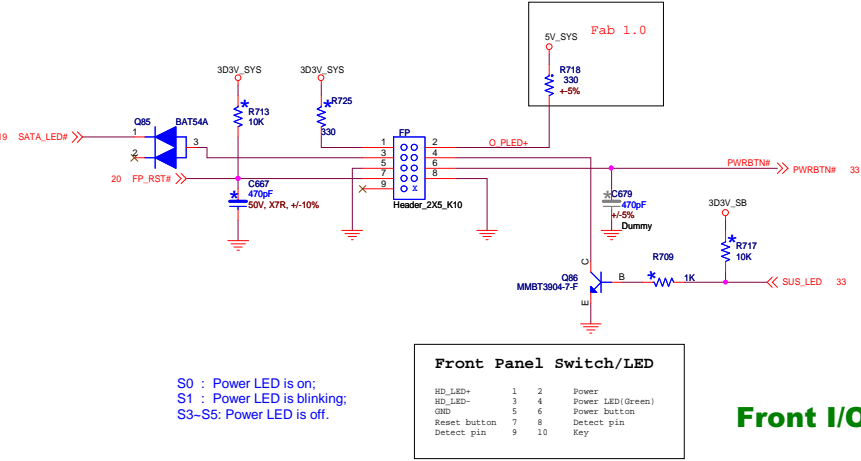
ATX POWER CONNECTOR



BUZZER/Speaker Header

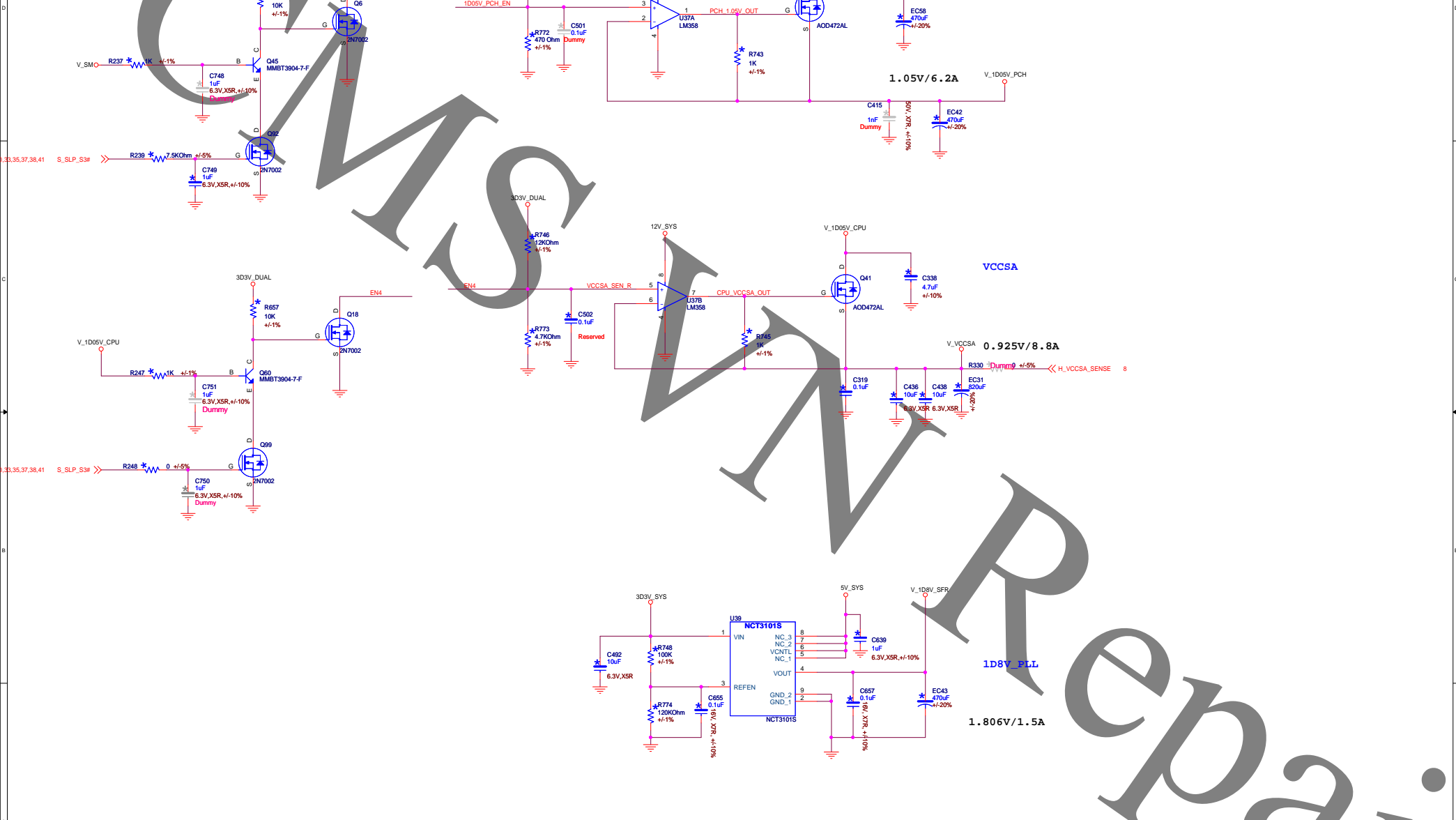


Front I/O Header



Front Panel Switch/LED			
HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(green)
GND	5	6	Power button
Reset button	7	8	Detect pin
Detect pin	9	10	Key

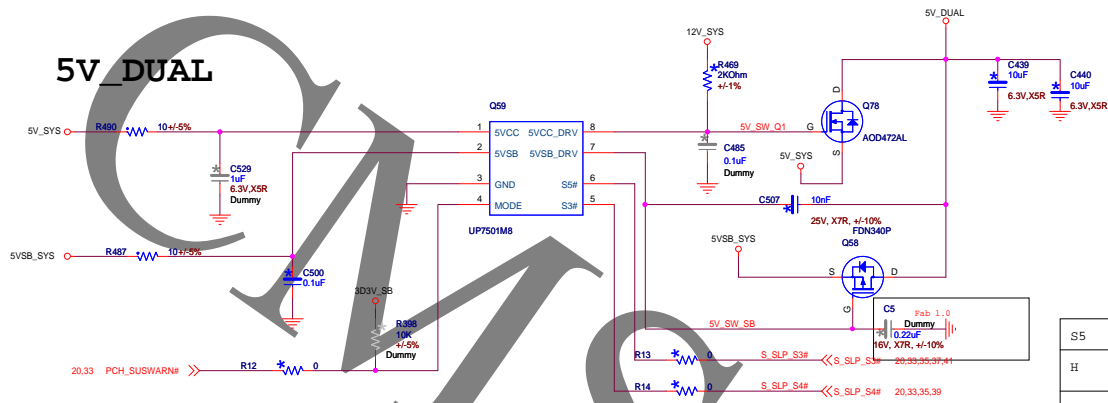
5	4	3	2	1
---	---	---	---	---



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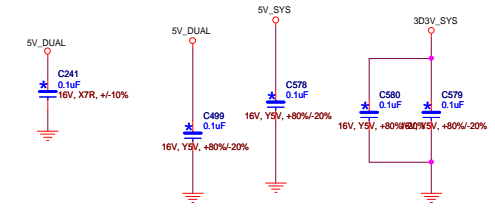


## 5V\_DUAL

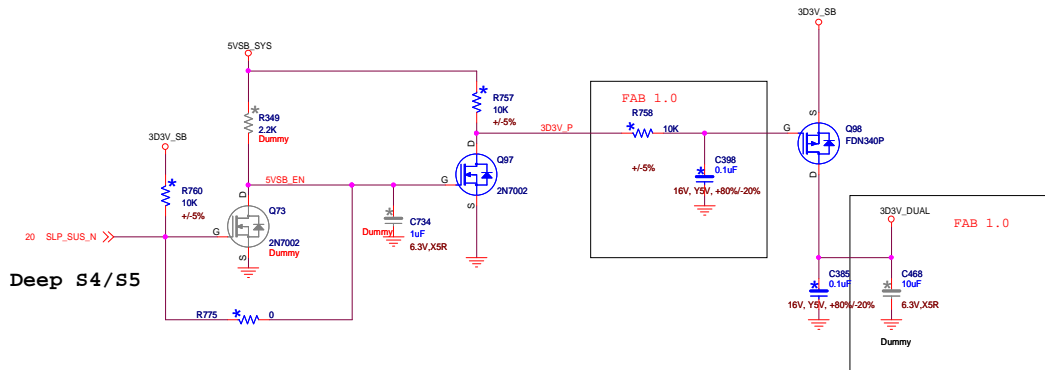


HI= S4/S5 5VDUAL FORM 5VSB  
Low= S4/S5 5VDUAL TURN OFF

S5	S3	NODE	5VDUAL
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

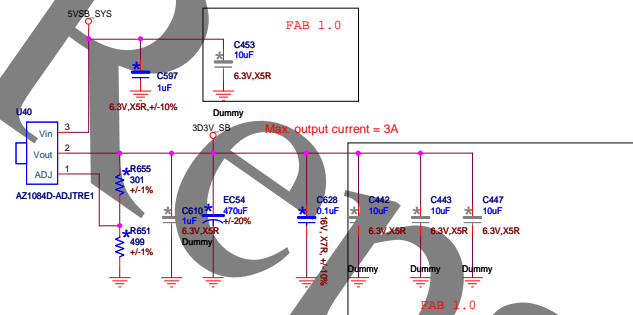


## 3D3V\_DUAL



Deep S4/S5

## 3D3V\_SB



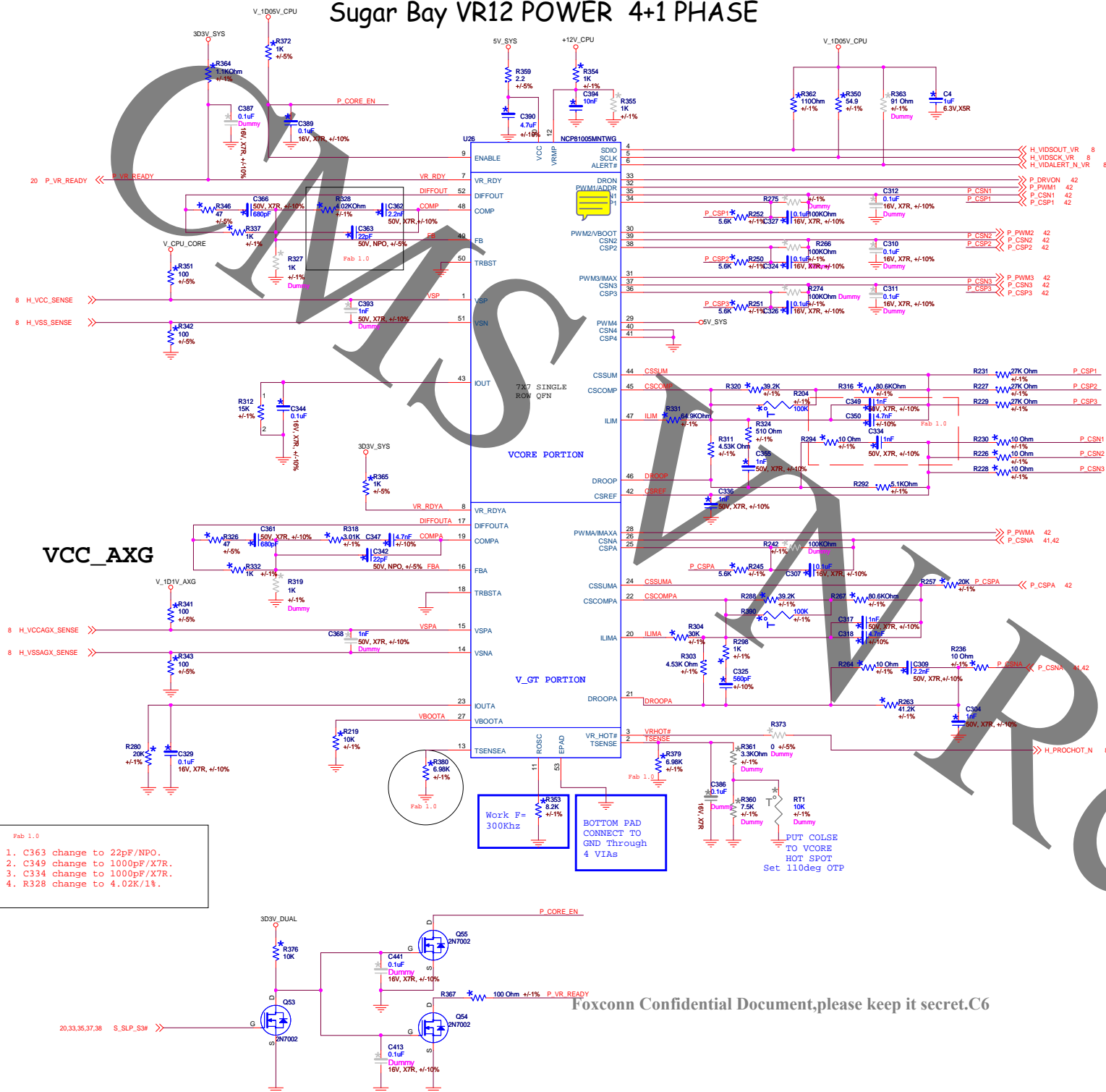
$V_{out} = V_{ref} (1 + R2/R1) + I_{adj} R2$   
R1 is Up Resistor.  
 $I_{adj} = 50\mu A$   
 $V_{ref} = 1.25V$

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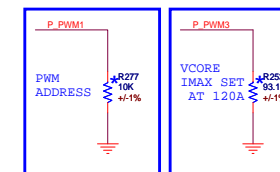
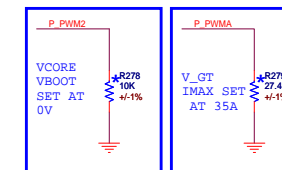




# Sugar Bay VR12 POWER 4+1 PHASE

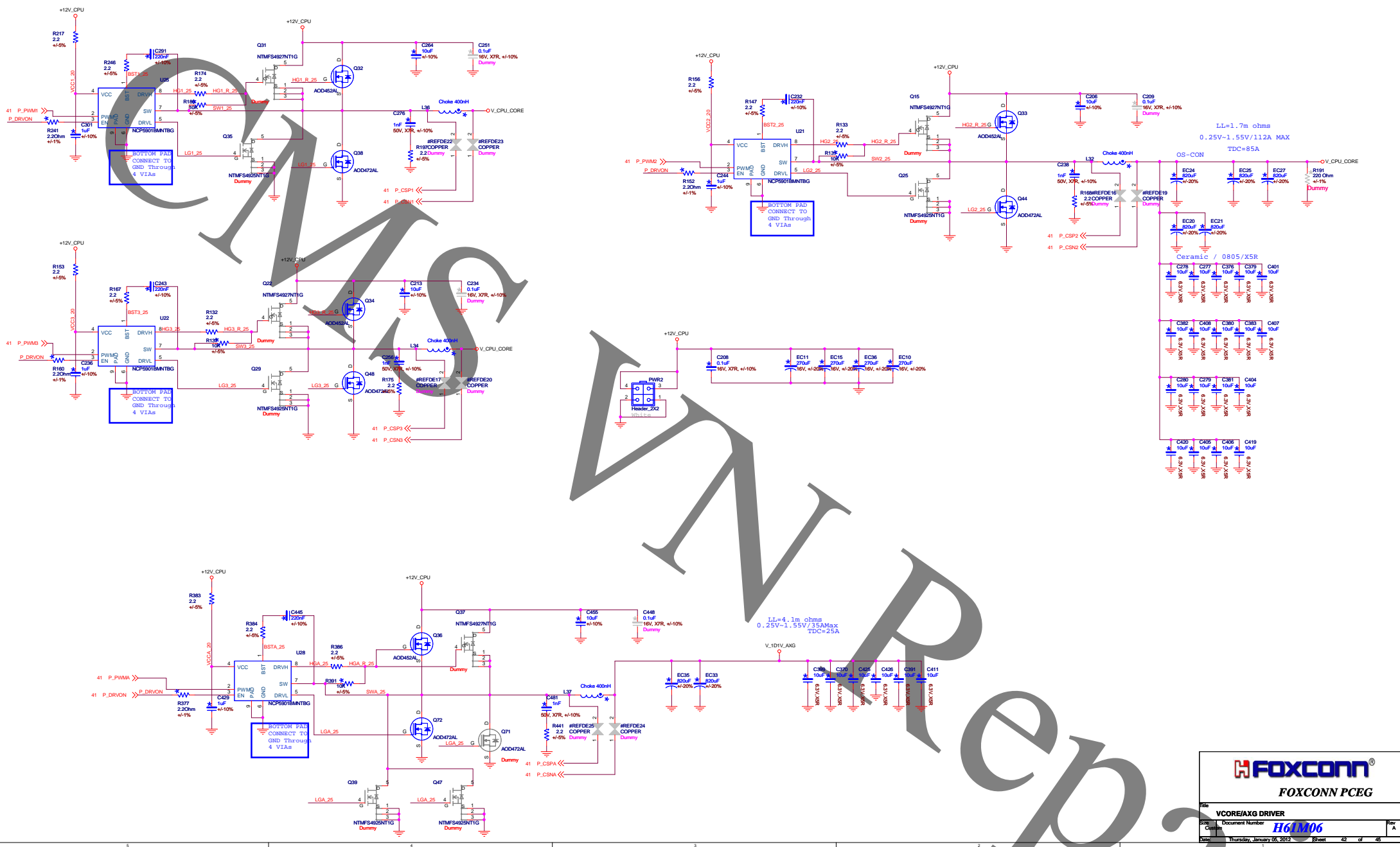


VCC\_CORE



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1.0V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V

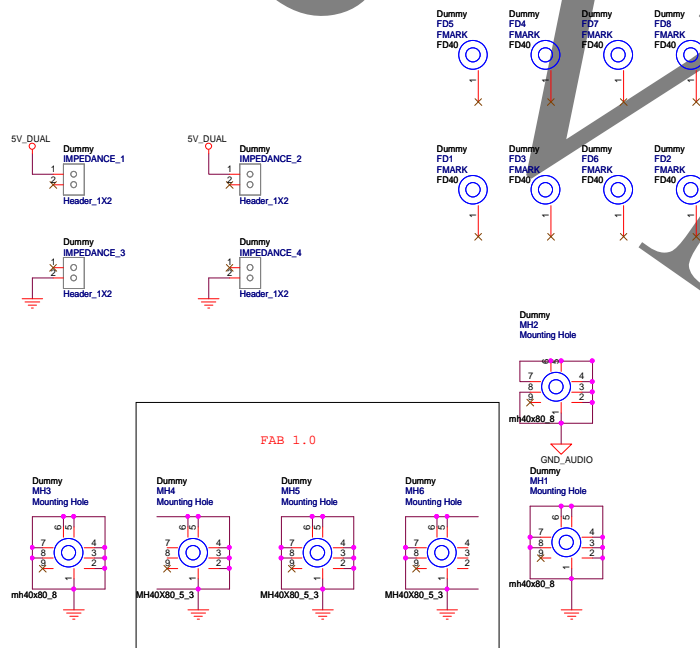
PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101



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Vcore/AXG DRIVER		
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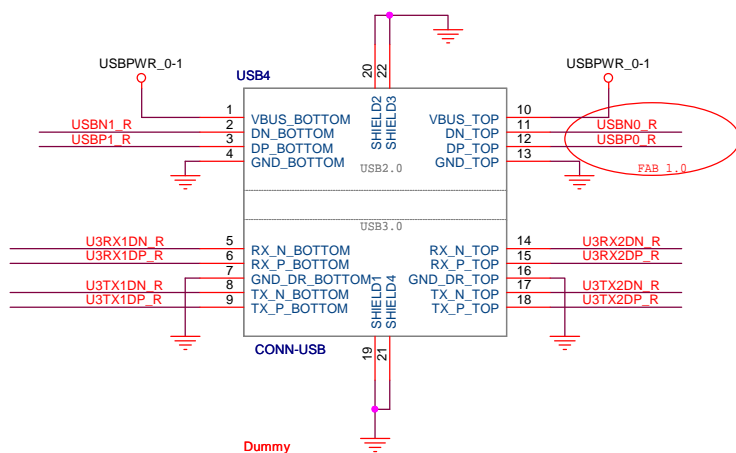
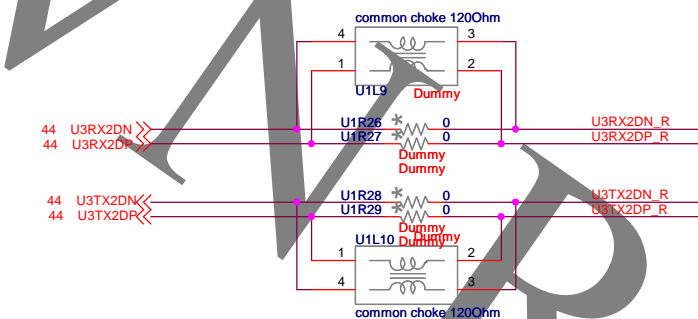
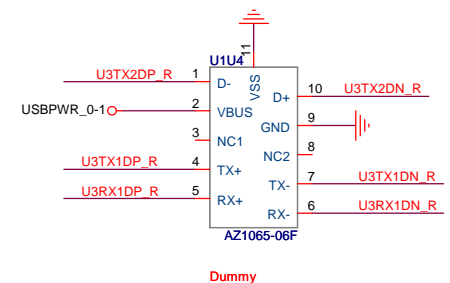
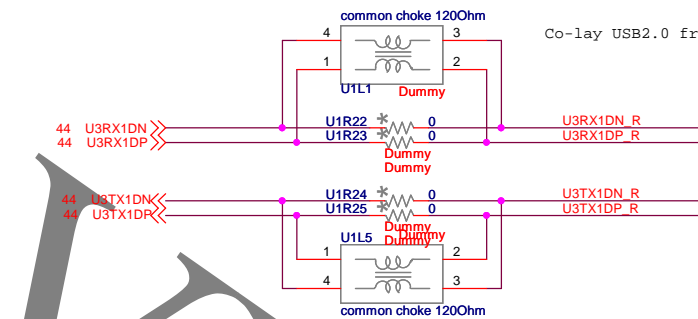
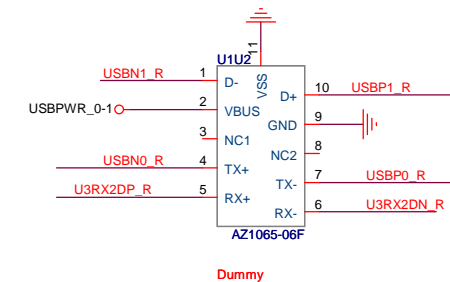
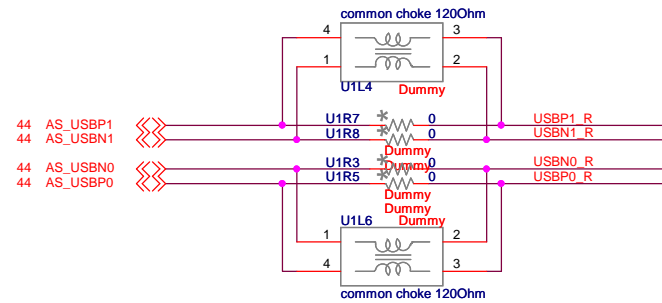
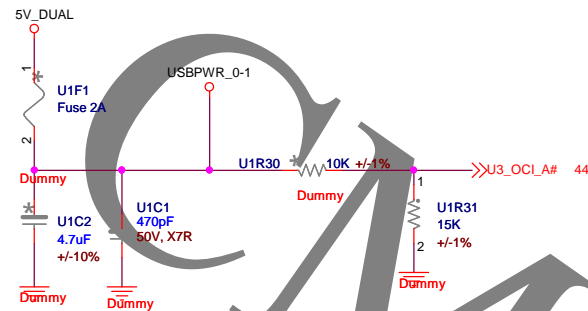
CMS




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<b>FOXCONN®</b> <b>FOXCONN PCEG</b>		
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